

Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Attorney Docket No: U.S. ARTCP012C 10/026,245 Applicant: S. Becker Filing Date: December 17, 2001 Group: 2123
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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
<i>W</i>	A	35,154	02/1996	Hardee	365	189.09
<i>W</i>	B	35,430	01/1997	Yamada et al.	365	189.01
<i>W</i>	C	4,418,403	11/1983	O'Toole et al.	365	201
<i>W</i>	D	4,432,076	02/1984	Yamada et al.	365	190
<i>W</i>	E	4,663,740	05/1987	Ebel	365	185
<i>W</i>	F	4,694,425	09/1987	Imel	365	49
<i>W</i>	G	4,791,613	12/1988	Hardee	365	189
<i>W</i>	H	4,858,182	08/1989	Pang et al.	365	156
<i>W</i>	I	4,873,664	10/1989	Eaton, Jr.	365	145
<i>W</i>	J	4,894,804	01/1990	Uchida	365	190
<i>W</i>	K	4,916,661	04/1990	Nawaki et al.	365	51

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
<i>W</i>	L	JP 1-112590	1989/5/1	JPO	G11C	11/34	X	
<i>W</i>	M	JP 1-133285	1989/5/25	JPO	G11C	11/34	X	
<i>W</i>	N	JP 4-349293	1992/12/3	JPO	G11C	11/401	X	
<i>W</i>	O	JP 6-251580	1994/9/9	JPO	G11C	11/401	X	
<i>W</i>	P	JP 6-28862	1994/2/4	JPO	G11C	11/41	X	

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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
<i>W</i>	Q	Katsunori et al., "9-ns 16-Mb CMOS SRAM with offset-compensated current sense amplifier", 11/1993, p. 1119-1124, IEEE Journal of Solid-State Circuits, v. 28 n, Sony Corp., Japan.
<i>W</i>	R	Yamauchi et al., "A 0.5 V/100 MHz over-V/sub CC/grounded data storage (OVGS) SRAM cell architecture with boosted bit-line and offset source over-driving schemes", 8/1996, p. 49-54, IEEE Solid-State Circuits Council, New York, NY.
<i>W</i>	S	Watanabe et al., "Offset compensating bit-line sensing scheme for high density DRAM's", 1/1994, vol. 29, no. 1, p. 9-13, IEEE Journal of Solid-State Circuits, IBM Corp., NY.
Examiner: <i>W</i>		Date Considered: 8/12/04

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
<i>2</i>	A2	4,984,201	01/1991	Sato et al.	365	154
<i>2</i>	B2	5,040,144	08/1991	Pelley et al.	365	51
<i>2</i>	C2	5,058,073	10/1991	Cho et al.	365	205
<i>2</i>	D2	5,065,363	11/1991	Sato et al.	365	154
<i>2</i>	E2	5,166,902	11/1992	Silver	365	182
<i>2</i>	F2	5,237,533	08/1993	Papaliolios	365	207
<i>2</i>	G2	5,253,209	10/1993	Hoffmann et al.	365	201
<i>2</i>	H2	5,258,946	11/1993	Graf	365	49
<i>2</i>	I2	5,289,432	02/1994	Dhong et al.	365	230.05
<i>2</i>	J2	5,297,089	03/1994	Wong	365	202
<i>2</i>	K2	5,305,252	04/1994	Saeki	365	63

Foreign Patent or Published Foreign Patent Application

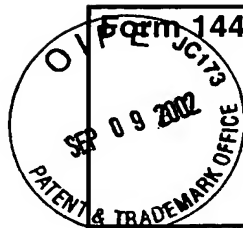
Examiner Initial	No.	Document No.	Date	Country or Patent Office	Class	Sub-class	Translation <i>ABSTRACT</i>	
							Yes	No
<i>2</i>	L2	JP 4-372789	1992/12/25	JPO	G11C	11/401	X	
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Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
<i>2</i>	Q2	Kraus et al., "Optimized sensing scheme of DRAMs", 8/1989, IEEE Journal of Solid-State Circuits, vol. 24, no. 4, p.895-9, USA.
<i>2</i>	R2	Chou et al., "A 60-ns 16-Mbit DRAM with a Minimized Sensing Delay Caused by Bit-Line Stray Capacitance", 10/1989, IEEE Journal of Solid-State Circuits, vol. 24, no. 5, p. 1176-1183, Japan.
<i>2</i>	S2	Taylor et al., "A 1Mb CMOS DRAM with a Divided Bitline Matrix Architecture", 2/1985, IEEE International Solid-State Circuits Conf., Carrolton, TX.
Examiner <i>202</i>	Date Considered <i>2/12/04</i>	

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
~	A3	5,410,505	04/1995	Furuyama	365	189.05
~	B3	5,434,821	07/1995	Watanabe et al.	365	203
~	C3	5,475,638	12/1995	Anami et al.	365	189.11
~	D3	5,487,029	01/1996	Kuroda	365	145
~	E3	5,555,212	09/1996	Toshiaki et al.	365	200
~	F3	5,581,126	12/1996	Moench	257	776
~	G3	5,644,525	07/1997	Takashima et al.	365	51
~	H3	5,671,174	09/1997	Koike et al.	365	145
~	I3	5,677,887	10/1997	Ishibashi et al.	365	205
~	J3	5,729,492	03/1998	Campardo	365	185.21
~	K3	5,745,402	04/1998	Arase	365	145

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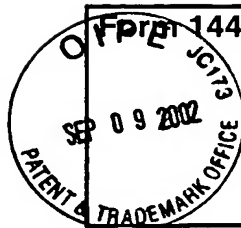
Examiner Initial	No.	Document No.	Date	Country or Patent Office	Class	Sub-class	Translation	
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Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
~	Q3	Yoshihara et al., "A Twisted Bit Line Technique for Multi-Mb DRAMs", 2/1988, Mitsubishi LSI Research and Development Laboratory, Itami, Japan.
3	R3	Taylor et al., "A 1-Mbit CMOS Dynamic RAM with a Divided Bitline Matrix Architecture", 10/1985, IEEE Journal of Solid-State Circuits, vol. Sc-20, no. 5, p. 894-902, Carrollton, TX.
	S	
Examiner <i>~</i>		Date Considered <i>8/12/02</i>

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JPPT 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)		Attorney Docket No: U.S. ARTCP012C 10/026,245 Applicant: S. Becker Filing Date: December 17, 2001 Group: 2123
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U.S. Patent Documents

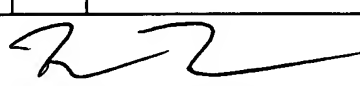
Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
~	A4	5,745,420	04/1998	McClure	365	201
~	B4	5,754,488	05/1998	Suh	365	205
~	C4	5,768,182	06/1998	Hu et al.	365	145
~	D4	5,796,650	08/1998	Wik et al.	365	150
~	E4	5,801,983	09/1998	Saeki	365	149
~	F4	5,811,862	09/1998	Okugaki et al.	257	390
~	G4	5,862,092	01/1999	Hawkins et al.	365	221
~	H4	5,877,976	03/1999	Lattimore et al.	365	63
~	I4	5,917,754	06/1999	Pathak et al.	365	185.21
~	J4	5,930,185	07/1999	Wendell	365	201
~	K4	5,982,666	11/1999	Campardo	365	185.21

Foreign Patent or Published Foreign Patent Application

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Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
2	A5	5,986,923	11/1999	Zhang et al.	365	154
2	B5	6,072,732	06/2000	McClure	365	191
2	C5	6,075,725	06/2000	Choi et al.	365	185.2
2	D5	6,154,405	11/2000	Takemae et al.	365	210
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